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U.S. UTILITY Patent Application

PATENT NUMBER and
ISSUE DATE

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10085009	03/01/2002	438	129	2812	Q. Hoang

**APPLICANTS: Fukui Masahiro; Hayashi Naoki;

2818

**CONTINUING DATA VERIFIED:

NOTE my

** FOREIGN APPLICATIONS VERIFIED:

YES my

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RESCIND ☐

Foreign priority claimed ☒ yes ☐ no

35 USC 119 conditions met ☒ yes ☐ no

Verified and Acknowledged Examiners's initials *mm*

ATTORNEY DOCKET NO

60188-156

TITLE : Wiring method in layout design of semiconductor integrated circuit, semiconductor integrated circuit and functional macro

U.S. DEPT. OF COMM./PAT. & TM.-PTO-435L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
Assistant Examiner		DRAWING	
ISSUE FEE		Sheet(s) Draw.	Fig(s) Draw.
Amount Due	Date Paid	Print Fig.	
Primary Examiner		Applicant's Examiner	
<input type="checkbox"/> TERMINAL DISCLAIMER		PREPARED FOR ISSUE	
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